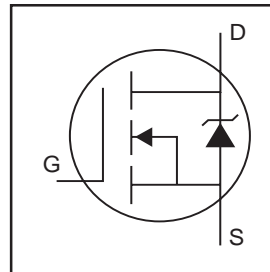


Features

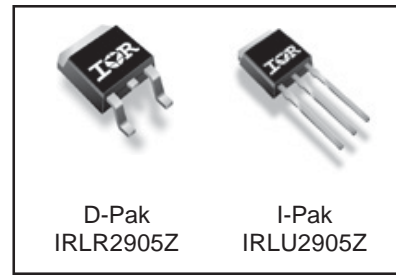
- Logic Level
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free



| |
|----------------------------|
| $V_{DSS} = 55V$ |
| $R_{DS(on)} = 13.5m\Omega$ |
| $I_D = 42A$ |

Description

Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.



Absolute Maximum Ratings

| | Parameter | Max. | Units |
|------------------------------|--|--------------------------|-------|
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited) | 60 | A |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 43 | |
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited) | 42 | |
| I_{DM} | Pulsed Drain Current ① | 240 | |
| $P_D @ T_C = 25^\circ C$ | Power Dissipation | 110 | W |
| | Linear Derating Factor | 0.72 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 16 | V |
| E_{AS} (Thermally limited) | Single Pulse Avalanche Energy ② | 57 | mJ |
| E_{AS} (Tested) | Single Pulse Avalanche Energy Tested Value ③ | 85 | |
| I_{AR} | Avalanche Current ① | See Fig.12a, 12b, 15, 16 | A |
| E_{AR} | Repetitive Avalanche Energy ④ | | mJ |
| T_J | Operating Junction and Storage Temperature Range | -55 to + 175 | °C |
| T_{STG} | | | |
| | | | |
| | Mounting Torque, 6-32 or M3 screw | 10 lbf•in (1.1N•m) | |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|-----------------|-------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case ⑤ | — | 1.38 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount) ⑥ ⑦ | — | 40 | |
| $R_{\theta JA}$ | Junction-to-Ambient ⑧ | — | 110 | |

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--|--------------------------------------|------|-------|------|-------|---|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 55 | — | — | V | V _{GS} = 0V, I _D = 250μA |
| ΔV _{(BR)DSS} /ΔT _J | Breakdown Voltage Temp. Coefficient | — | 0.053 | — | V/°C | Reference to 25°C, I _D = 1mA |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | 11 | 13.5 | mΩ | V _{GS} = 10V, I _D = 36A ③ |
| | | — | — | 20 | mΩ | V _{GS} = 5.0V, I _D = 30A ③ |
| | | — | — | 22.5 | mΩ | V _{GS} = 4.5V, I _D = 15A ③ |
| V _{GS(th)} | Gate Threshold Voltage | 1.0 | — | 3.0 | V | V _{DS} = V _{GS} , I _D = 250μA |
| g _{fs} | Forward Transconductance | 25 | — | — | S | V _{DS} = 25V, I _D = 36A |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | 20 | μA | V _{DS} = 55V, V _{GS} = 0V |
| | | — | — | 250 | μA | V _{DS} = 55V, V _{GS} = 0V, T _J = 125°C |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | 200 | nA | V _{GS} = 16V |
| | Gate-to-Source Reverse Leakage | — | — | -200 | nA | V _{GS} = -16V |
| Q _g | Total Gate Charge | — | 23 | 35 | nC | I _D = 36A |
| Q _{gs} | Gate-to-Source Charge | — | 8.5 | — | nC | V _{DS} = 44V |
| Q _{gd} | Gate-to-Drain ("Miller") Charge | — | 12 | — | nC | V _{GS} = 5.0V ③ |
| t _{d(on)} | Turn-On Delay Time | — | 14 | — | ns | V _{DD} = 28V |
| t _r | Rise Time | — | 130 | — | ns | I _D = 36A |
| t _{d(off)} | Turn-Off Delay Time | — | 24 | — | ns | R _G = 15 Ω |
| t _f | Fall Time | — | 33 | — | ns | V _{GS} = 5.0V ③ |
| L _D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| L _S | Internal Source Inductance | — | 7.5 | — | nH | |
| C _{iss} | Input Capacitance | — | 1570 | — | pF | V _{GS} = 0V |
| C _{oss} | Output Capacitance | — | 230 | — | pF | V _{DS} = 25V |
| C _{riss} | Reverse Transfer Capacitance | — | 130 | — | pF | f = 1.0MHz |
| C _{oss} | Output Capacitance | — | 840 | — | pF | V _{GS} = 0V, V _{DS} = 1.0V, f = 1.0MHz |
| C _{oss} | Output Capacitance | — | 180 | — | pF | V _{GS} = 0V, V _{DS} = 44V, f = 1.0MHz |
| C _{oss eff.} | Effective Output Capacitance | — | 290 | — | pF | V _{GS} = 0V, V _{DS} = 0V to 44V ④ |

Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|-----------------|---|--|------|------|-------|---|
| I _S | Continuous Source Current (Body Diode) | — | — | 42 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I _{SM} | Pulsed Source Current (Body Diode) ① | — | — | 240 | A | |
| V _{SD} | Diode Forward Voltage | — | — | 1.3 | V | T _J = 25°C, I _S = 36A, V _{GS} = 0V ③ |
| t _{rr} | Reverse Recovery Time | — | 22 | 33 | ns | T _J = 25°C, I _F = 36A, V _{DD} = 28V |
| Q _{rr} | Reverse Recovery Charge | — | 14 | 21 | nC | di/dt = 100A/μs ③ |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

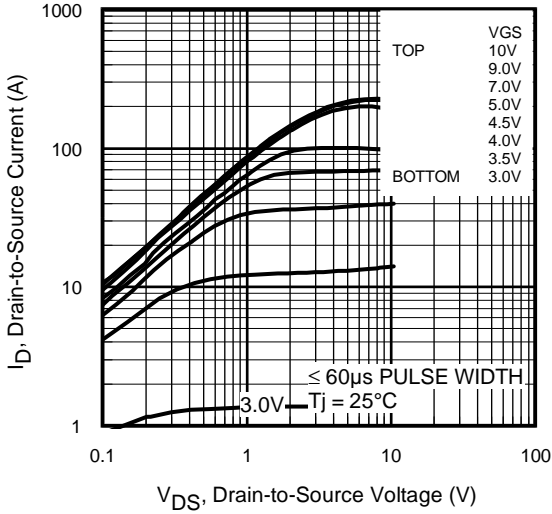


Fig 1. Typical Output Characteristics

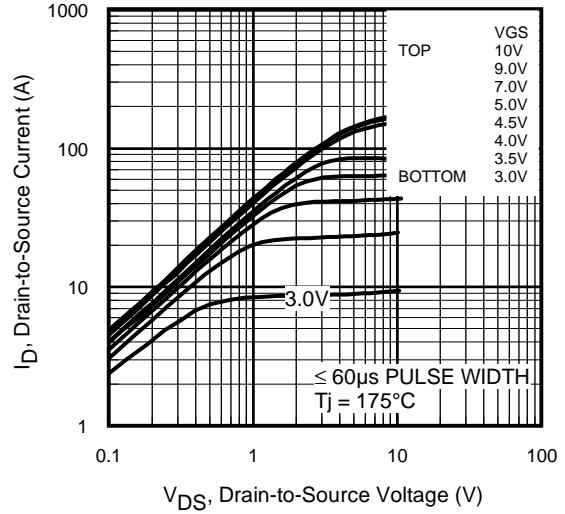


Fig 2. Typical Output Characteristics

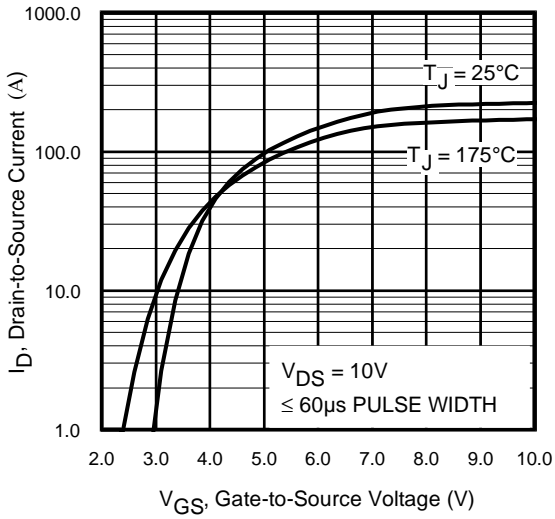


Fig 3. Typical Transfer Characteristics

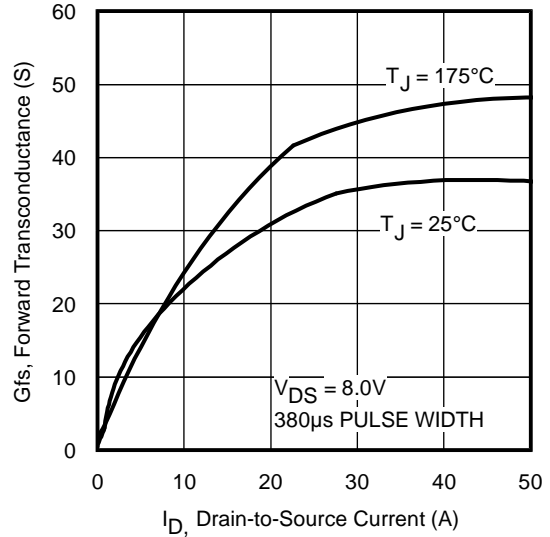


Fig 4. Typical Forward Transconductance Vs. Drain Current

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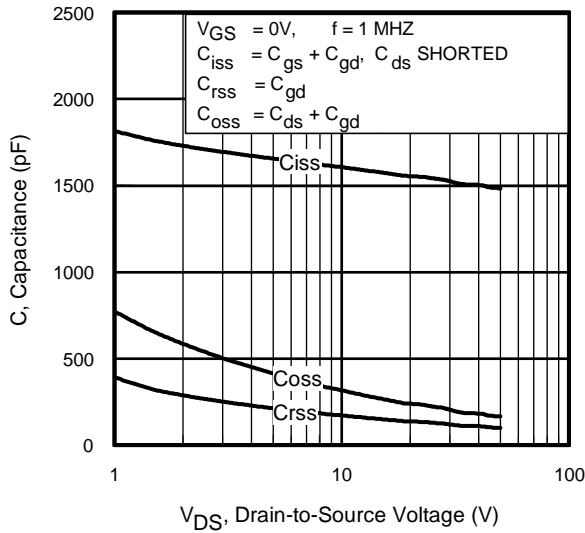


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

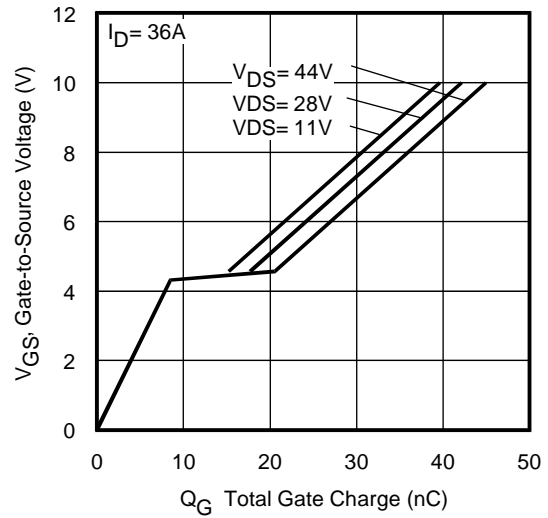


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

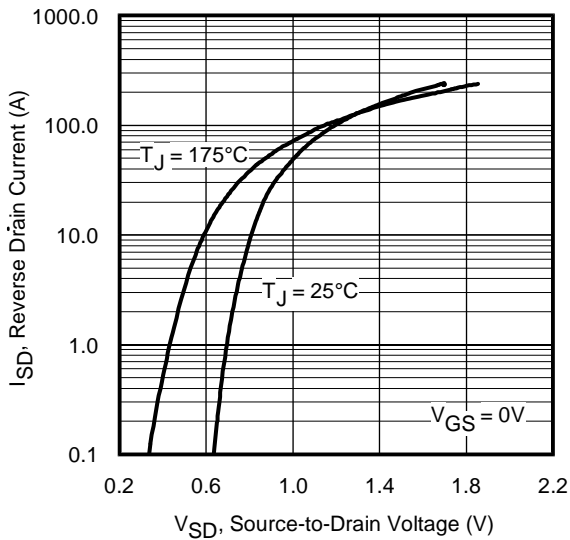


Fig 7. Typical Source-Drain Diode Forward Voltage

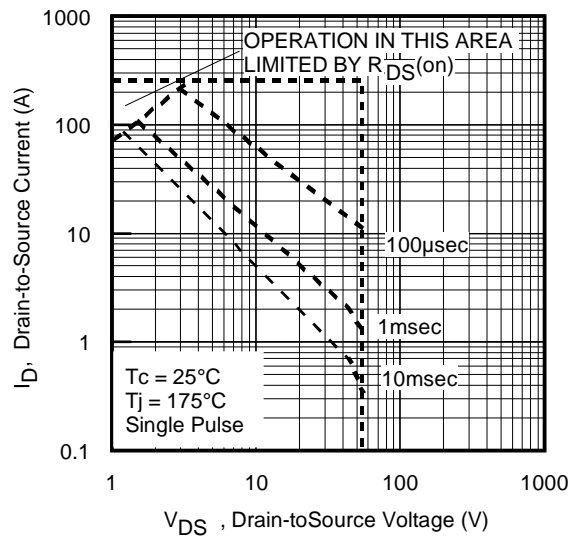


Fig 8. Maximum Safe Operating Area

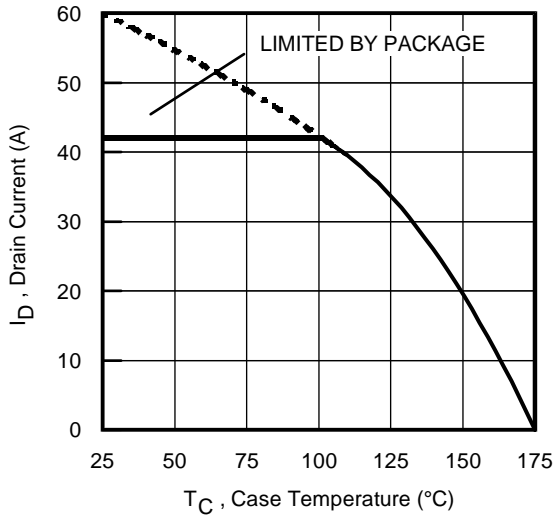


Fig 9. Maximum Drain Current Vs. Case Temperature

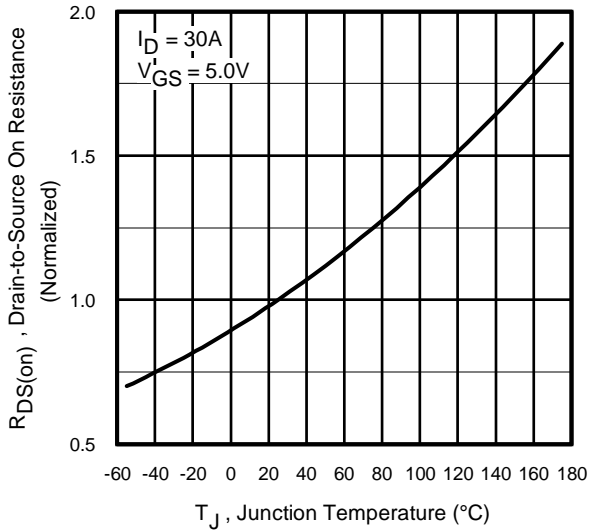


Fig 10. Normalized On-Resistance Vs. Temperature

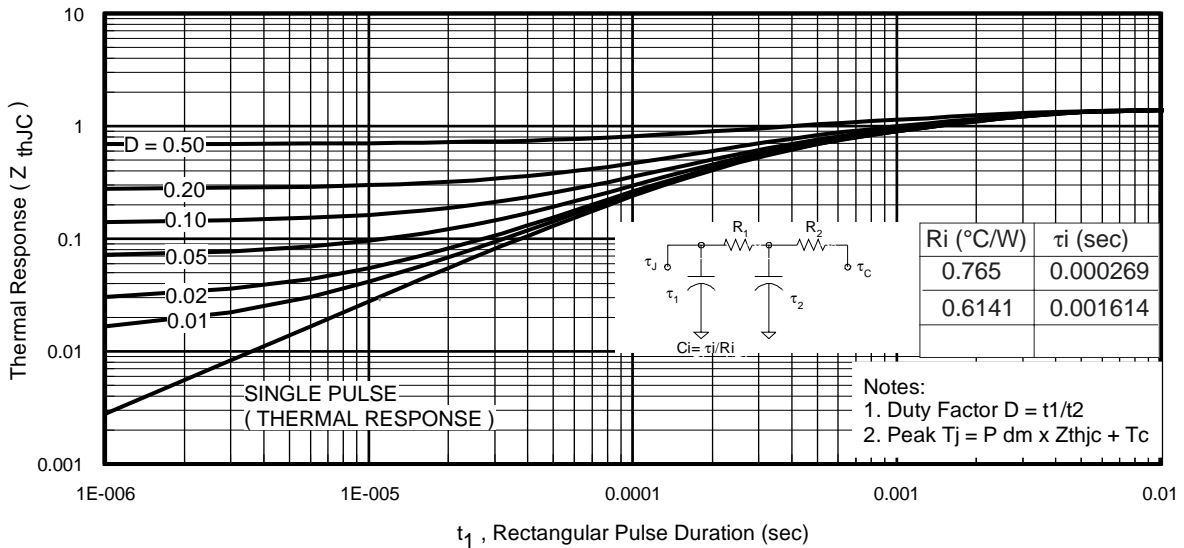


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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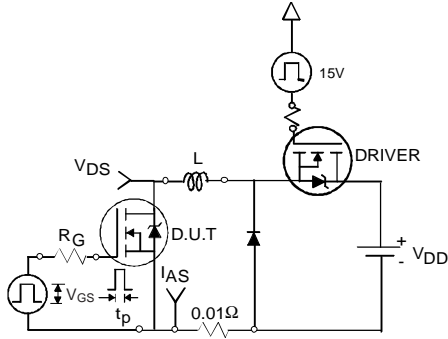


Fig 12a. Unclamped Inductive Test Circuit



Fig 12b. Unclamped Inductive Waveforms

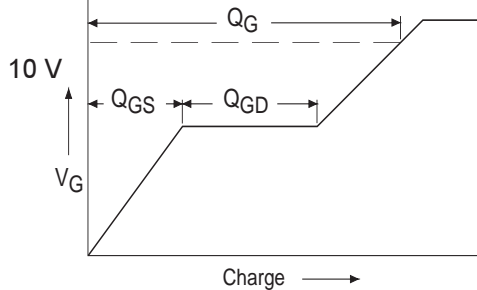


Fig 13a. Basic Gate Charge Waveform

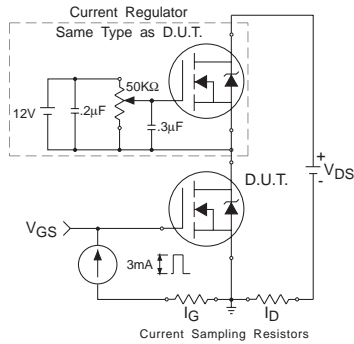


Fig 13b. Gate Charge Test Circuit

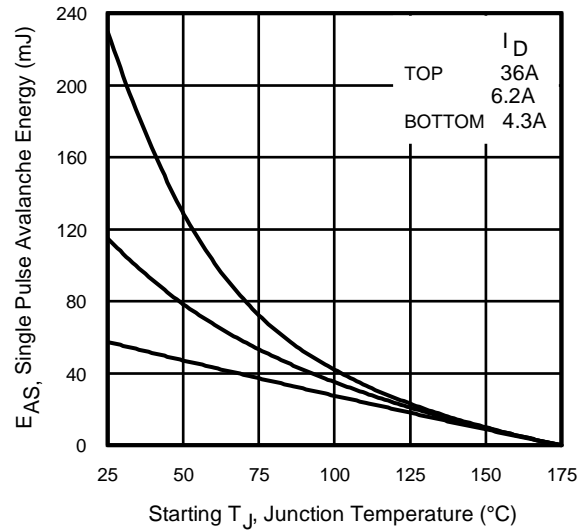


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

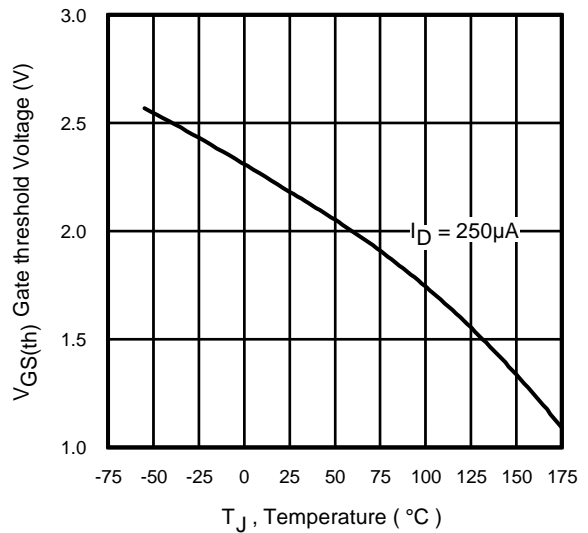


Fig 14. Threshold Voltage Vs. Temperature

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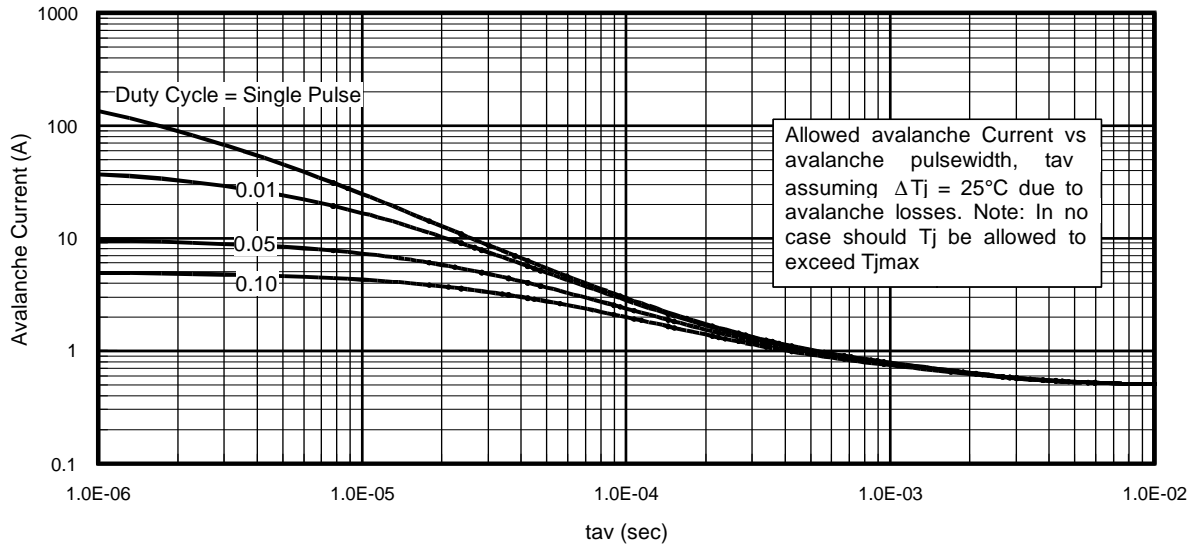


Fig 15. Typical Avalanche Current Vs.Pulsewidth

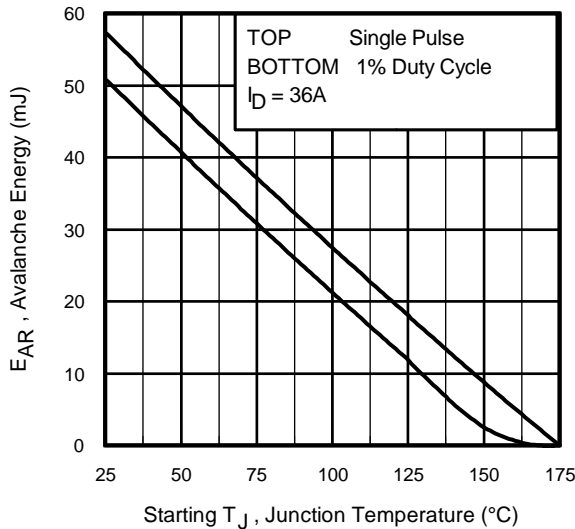


Fig 16. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 15, 16:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 15, 16).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

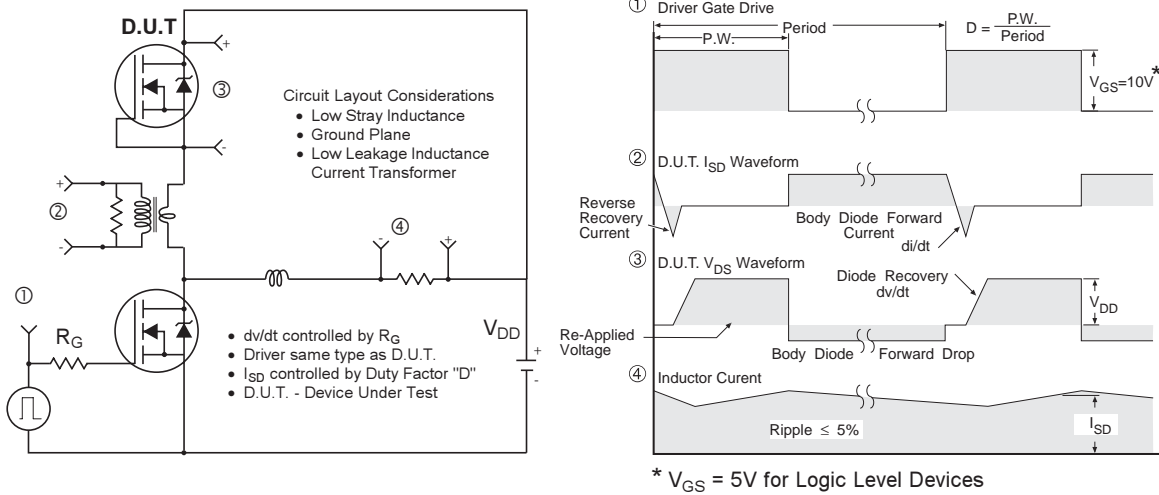


Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

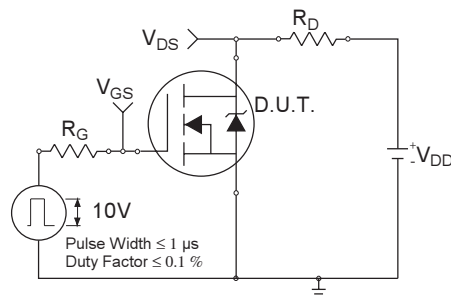


Fig 18a. Switching Time Test Circuit

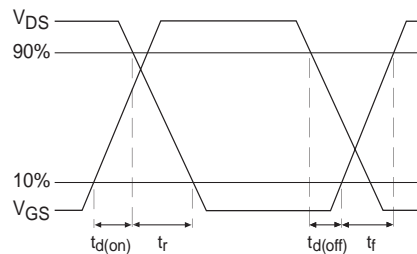
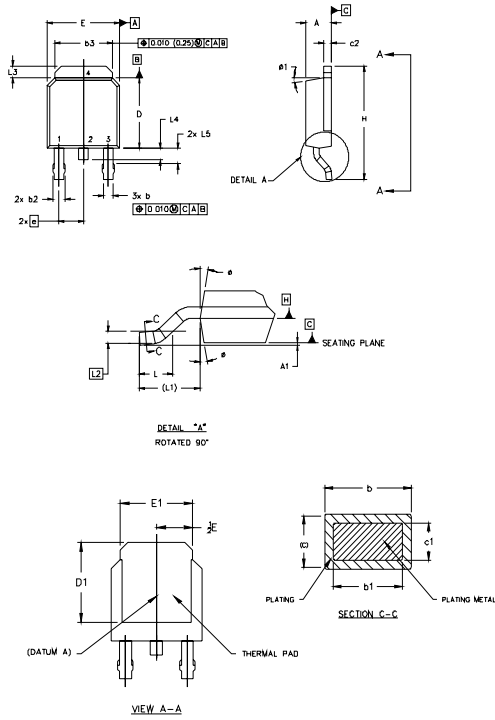


Fig 18b. Switching Time Waveforms

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.0 LEAD DIMENSION UNCONTROLLED IN L5
- 4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.0 SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540] FROM THE LEAD TIP.
- 6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|-----------|-------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | |
| A1 | | 0.13 | | .005 | |
| b | 0.64 | 0.89 | .025 | .035 | 5 |
| b1 | 0.64 | 0.79 | .025 | 0.031 | 5 |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 4.95 | 5.46 | .195 | .215 | |
| c | 0.46 | 0.61 | .018 | .024 | 5 |
| c1 | 0.41 | 0.56 | .016 | .022 | 5 |
| c2 | .046 | 0.89 | .018 | .035 | 5 |
| D | 5.97 | 6.22 | .235 | .245 | 6 |
| D1 | 5.21 | - | .205 | - | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 6 |
| E1 | 4.32 | - | .170 | - | 4 |
| e | 2.29 | | .090 BSC | | |
| H | 9.40 | 10.41 | .570 | .410 | |
| L | 1.40 | 1.78 | .055 | .070 | |
| L1 | 2.74 REF. | | .108 REF. | | |
| L2 | 0.051 BSC | | .020 BSC | | |
| L3 | 0.89 | 1.27 | .035 | .050 | |
| L4 | | 1.02 | | .040 | |
| L5 | 1.14 | 1.52 | .045 | .060 | 3 |
| Ø | 0" | 10" | 0" | 10" | |
| Ø1 | 0" | 15" | 0" | 15" | |

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

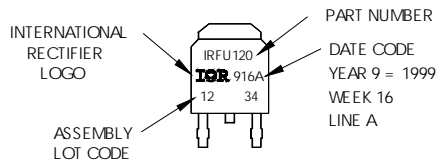
IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

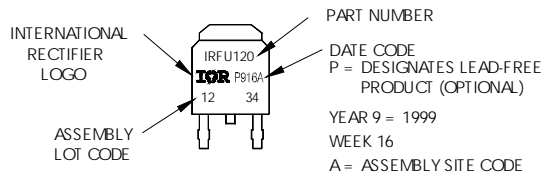
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"



OR

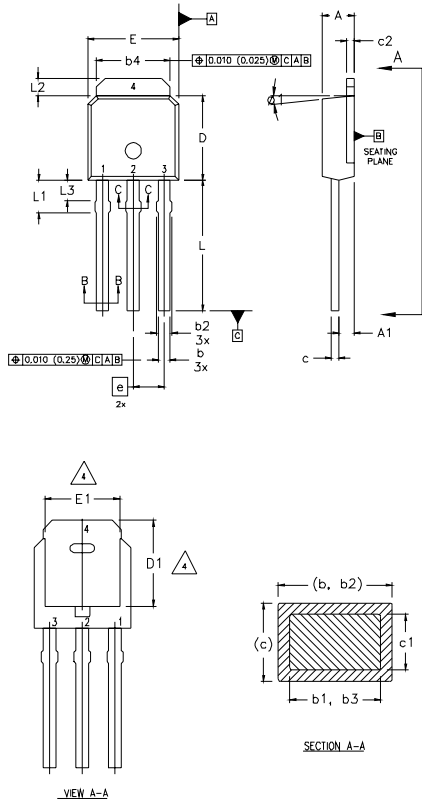


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IR Rectifier

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.008" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
- 5 LEAD DIMENSION UNCONTROLLED IN L3.
- 6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
- 7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
- 8 CONTROLLING DIMENSION : INCHES.

LEAD ASSIGNMENTS

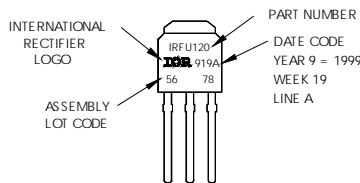
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

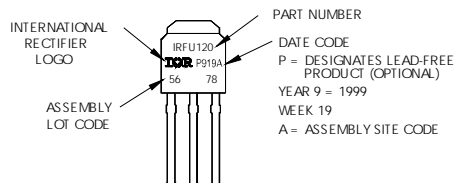
| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|------|-----------|-------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | 0.086 | .094 | |
| A1 | 0.89 | 1.14 | 0.035 | 0.045 | |
| b | 0.64 | 0.89 | 0.025 | 0.035 | |
| b1 | 0.64 | 0.79 | 0.025 | 0.031 | 4 |
| b2 | 0.76 | 1.14 | 0.030 | 0.045 | |
| b3 | 0.76 | 1.04 | 0.030 | 0.041 | |
| b4 | 5.00 | 5.46 | 0.195 | 0.215 | 4 |
| c | 0.46 | 0.61 | 0.018 | 0.024 | |
| c1 | 0.41 | 0.56 | 0.016 | 0.022 | |
| c2 | .046 | 0.86 | 0.018 | 0.035 | |
| D | 5.97 | 6.22 | 0.235 | 0.245 | 3, 4 |
| D1 | 5.21 | - | 0.206 | - | 4 |
| E | 6.35 | 6.73 | 0.250 | 0.265 | 3, 4 |
| E1 | 4.32 | - | 0.170 | - | 4 |
| e | 2.29 | | 0.090 BSC | | |
| L | 8.89 | 9.60 | 0.350 | 0.380 | |
| L1 | 1.91 | 2.29 | 0.075 | 0.090 | |
| L2 | 0.89 | 1.27 | 0.035 | 0.050 | 4 |
| L3 | 1.14 | 1.52 | 0.045 | 0.060 | 5 |
| Ø1 | Ø | 15' | Ø | 15' | |

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW19, 1999 IN THE ASSEMBLY LINE "A"
Note: "P" in assembly line position indicates "Lead-Free"

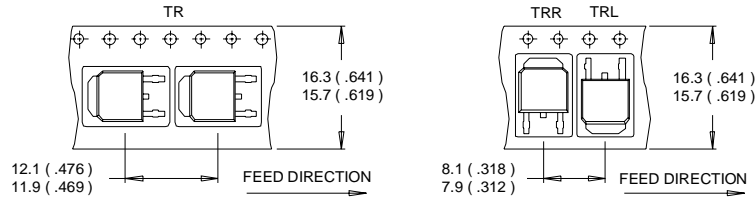


OR

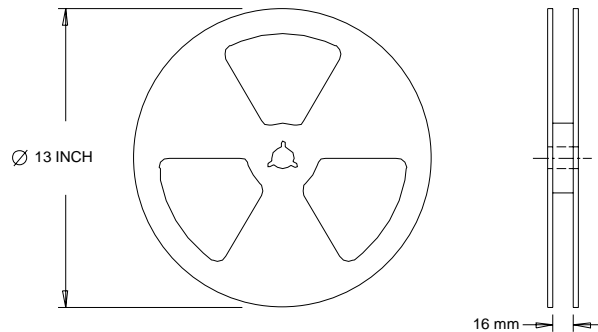


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES:
1. OUTLINE CONFORMS TO EIA-481.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T_{Jmax} ; starting $T_J = 25^\circ\text{C}$, $L = 0.089\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 36\text{A}$, $V_{GS} = 10\text{V}$. Part not recommended for use above this value.
- ③ Pulse width $\leq 1.0\text{ms}$; duty cycle $\leq 2\%$.
- ④ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑤ Limited by T_{Jmax} , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ R_θ is measured at T_J approximately 90°C

Data and specifications subject to change without notice.
This product has been designed for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.12/04