

The SN74LS16 is obsolete  
and is no longer supplied.

# SN54LS06, SN74LS06, SN74LS16 HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

SDLS020E – MAY 1990 – REVISED FEBRUARY 2004

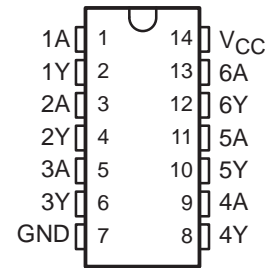
- Convert TTL Voltage Levels to MOS Levels
- High Sink-Current Capability
- Input Clamping Diodes Simplify System Design
- Open-Collector Driver for Indicator Lamps and Relays
- Inputs Fully Compatible With Most TTL Circuits

## description/ordering information

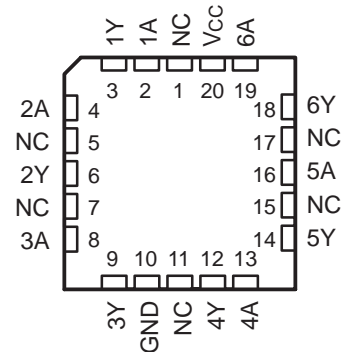
These hex inverter buffers/drivers feature high-voltage open-collector outputs to interface with high-level circuits (such as MOS), or for driving high-current loads, and also are characterized for use as inverter buffers for driving TTL inputs. The 'LS06 devices have a rated output voltage of 30 V, and the SN74LS16 has a rated output voltage of 15 V. The maximum sink current for the SN54LS06 is 30 mA, and for the SN74LS06 and SN74LS16 it is 40 mA.

These devices are compatible with most TTL families. Inputs are diode-clamped to minimize transmission effects, which simplifies design. Typical power dissipation is 175 mW, and average propagation delay time is 8 ns.

SN54LS06 . . . J PACKAGE  
SN74LS06, SN74LS16 . . . D, DB, N, OR NS PACKAGE  
(TOP VIEW)



SN54LS06 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74LS06N	SN74LS06N
	SOIC – D	Tube	SN74LS06D	LS06
		Tape and reel	SN74LS06DR	
	SOP – NS	Tape and reel	SN74LS06NSR	74LS06
	SSOP – DB	Tape and reel	SN74LS06DBR	LS06
–55°C to 125°C	CDIP – J	Tube	SN54LS06J	SN54LS06J
		Tube	SNJ54LS06J	SNJ54LS06J
	LCCC – FK	Tube	SNJ54LS06FK	SNJ54LS06FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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INSTRUMENTS**

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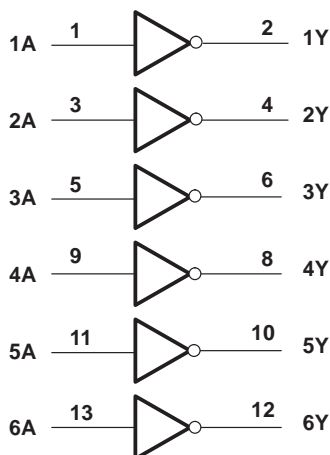
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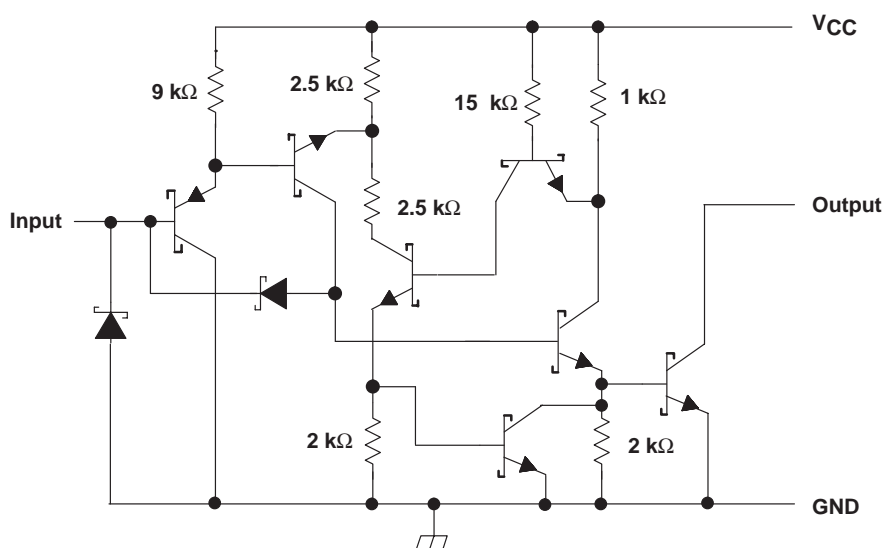
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## logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, and NS packages.

## schematic (each gate)



Resistor values shown are nominal.

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# SN54LS06, SN74LS06, SN74LS16

## HEX INVERTER BUFFERS/DRIVERS

### WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

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#### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC}$	7 V
Input voltage, $V_I$ (see Note 1)	7 V
Output voltage, $V_O$ (see Notes 1 and 2): SN54LS06, SN74LS06	30 V
SN74LS16	15 V
Package thermal impedance, $\theta_{JA}$ (see Note 3): D package	86°C/W
DB package	96°C/W
N package	80°C/W
NS package	76°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to GND.  
2. This is the maximum voltage that should be applied to any output when it is in the off state.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

#### recommended operating conditions (see Note 4)

			SN54LS06			SN74LS06 SN74LS16			UNIT	
			MIN	NOM	MAX	MIN	NOM	MAX		
V <sub>CC</sub>	Supply voltage		4.5	5	5.5	4.75	5	5.25	V	
V <sub>IH</sub>	High-level input voltage		2			2			V	
V <sub>IL</sub>	Low-level input voltage		0.8			0.8			V	
V <sub>OH</sub>	High-level output voltage	'LS06	30			30			V	
		SN74LS16				15				
I <sub>OL</sub>	Low-level output current		30			40			mA	
T <sub>A</sub>	Operating free-air temperature		−55			0			70	°C

NOTE 4: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

#### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS‡		SN54LS06			SN74LS06 SN74LS16			UNIT
			MIN	TYP§	MAX	MIN	TYP§	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = MIN, I <sub>I</sub> = –12 mA		–1.5			–1.5			V
I <sub>OH</sub>	V <sub>CC</sub> = MIN, V <sub>IL</sub> = 0.8 V	'LS06, V <sub>OH</sub> = 30 V	0.25			0.25			mA
		SN74LS16, V <sub>OH</sub> = 15 V				0.25			
V <sub>OL</sub>	V <sub>CC</sub> = MIN, V <sub>IH</sub> = 2 V	I <sub>OL</sub> = 16 mA	0.25	0.4		0.25	0.4	V	
		I <sub>OL</sub> = 30 mA	0.7						
		I <sub>OL</sub> = 40 mA			0.7				
I <sub>I</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7 V		1			1			mA
I <sub>IH</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.4 V		20			20			μA
I <sub>IL</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.4 V		–0.2			–0.2			mA
I <sub>CCH</sub>	V <sub>CC</sub> = MAX		18			18			mA
I <sub>CCL</sub>	V <sub>CC</sub> = MAX		60			60			mA

<sup>‡</sup> For conditions shown as MIN or MAX, use the appropriate value specified under *recommended operating conditions*.

<sup>§</sup> All typical values are at  $V_{CC} = 5 \text{ V}$ , and  $T_A = 25^\circ\text{C}$ .



**SN54LS06, SN74LS06, SN74LS16**  
**HEX INVERTER BUFFERS/DRIVERS**  
**WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS**

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switching characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
$t_{PLH}$	A	Y	$R_L = 110\ \Omega$ , $C_L = 15\text{ pF}$	7	15	ns
$t_{PHL}$				10	20	



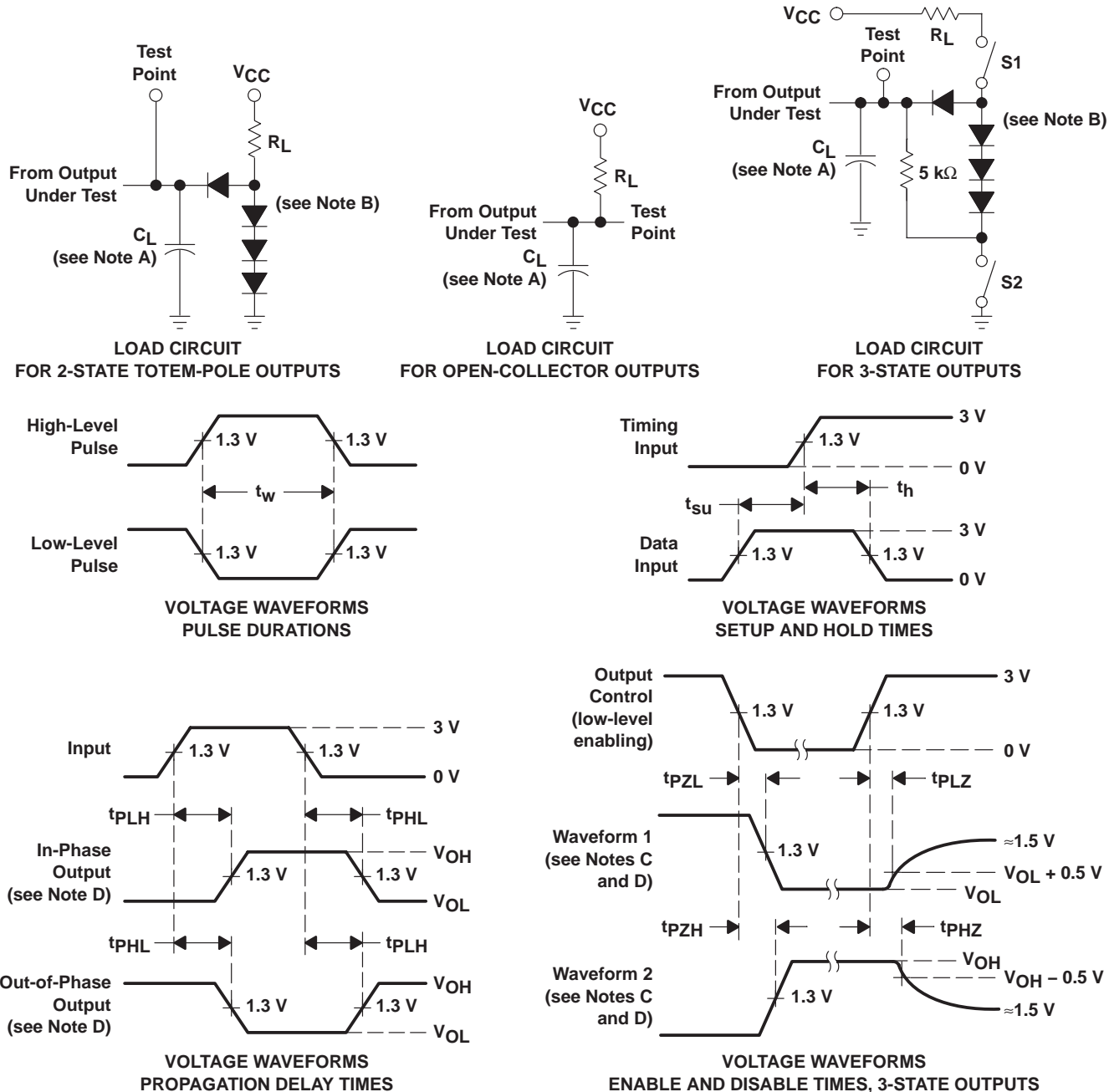
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# SN54LS06, SN74LS06, SN74LS16 HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

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## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - All diodes are 1N3064 or equivalent.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - S1 and S2 are closed for  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_{PHZ}$ , and  $t_{PLZ}$ ; S1 is open and S2 is closed for  $t_{PZH}$ ; S1 is closed and S2 is open for  $t_{PZL}$ .
  - Phase relationships between inputs and outputs have been chosen arbitrarily for these examples.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O \approx 50 \Omega$ ,  $t_r \leq 1.5$  ns,  $t_f \leq 2.6$  ns.
  - The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-9861701Q2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-9861701QCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN54LS06J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN74LS06D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS06DBLE	OBSOLETE	SSOP	DB	14		None	Call TI	Call TI
SN74LS06DBR	ACTIVE	SSOP	DB	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS06DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS06N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74LS06NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74LS16D	OBSOLETE	SOIC	D	14		None	Call TI	Call TI
SN74LS16DR	OBSOLETE	SOIC	D	14		None	Call TI	Call TI
SN74LS16N	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SNJ54LS06FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54LS06J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

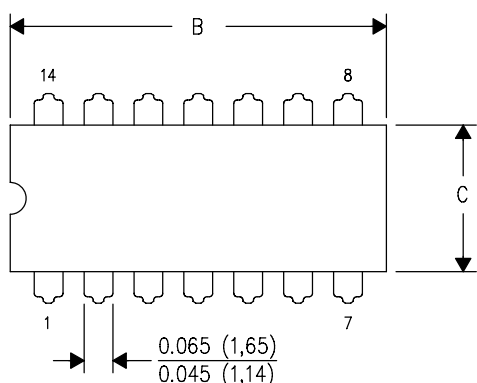
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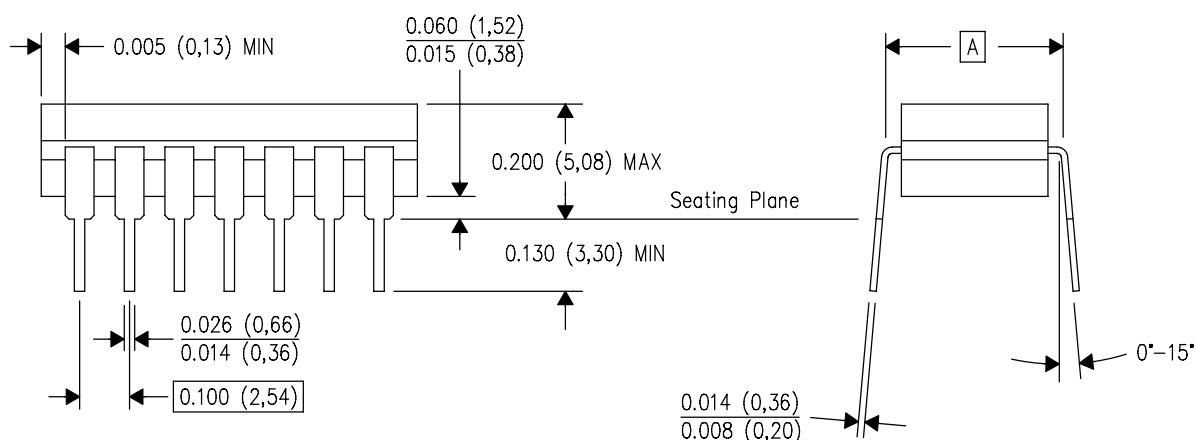
J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



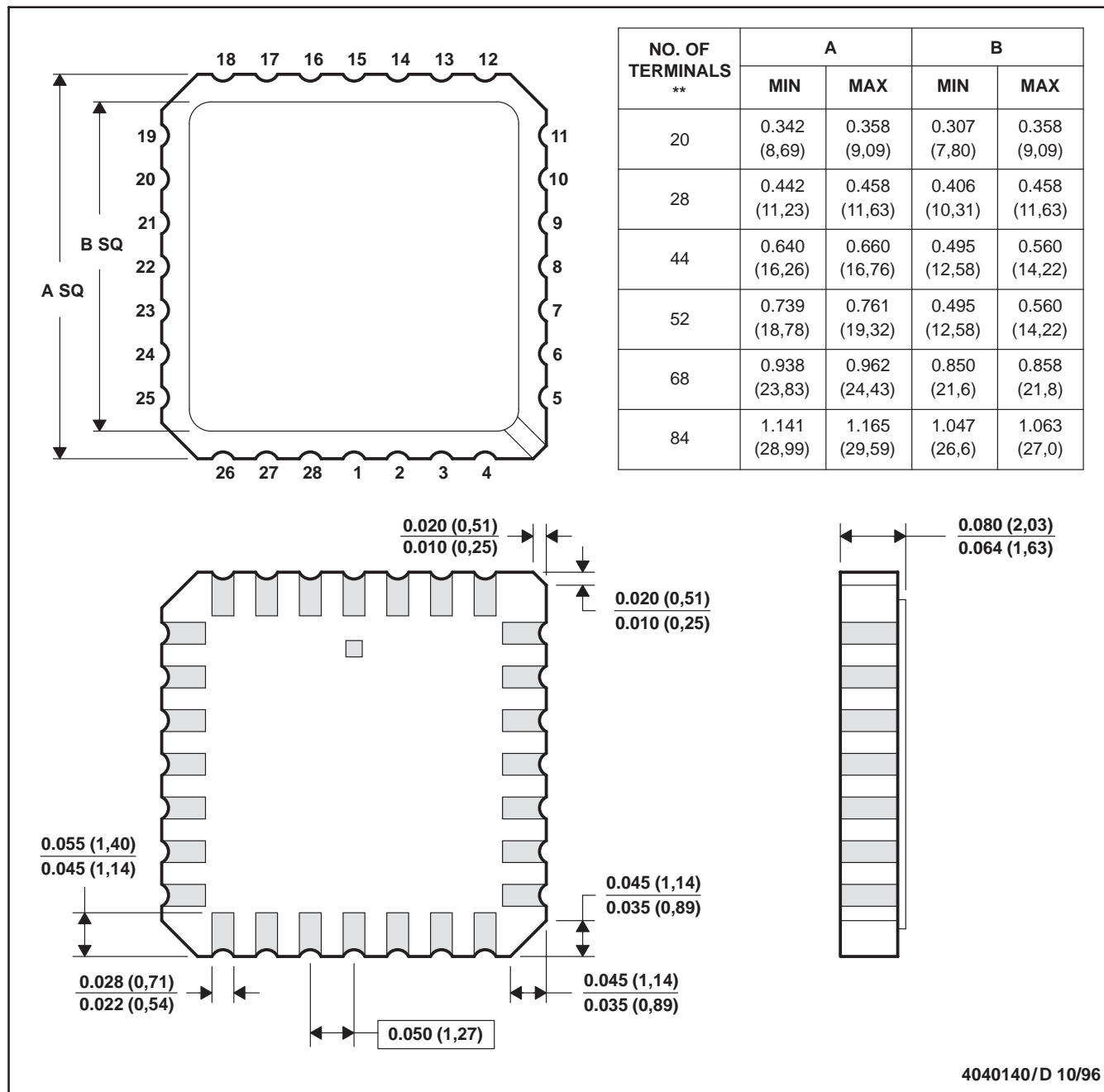
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



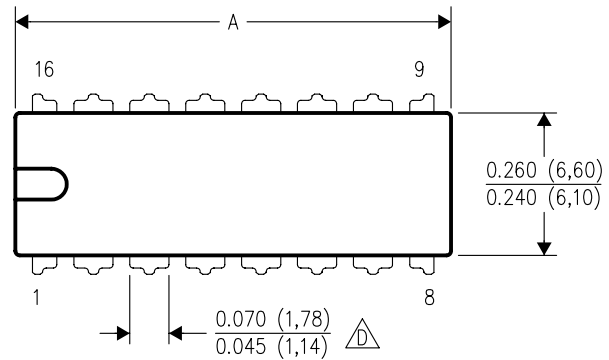
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004



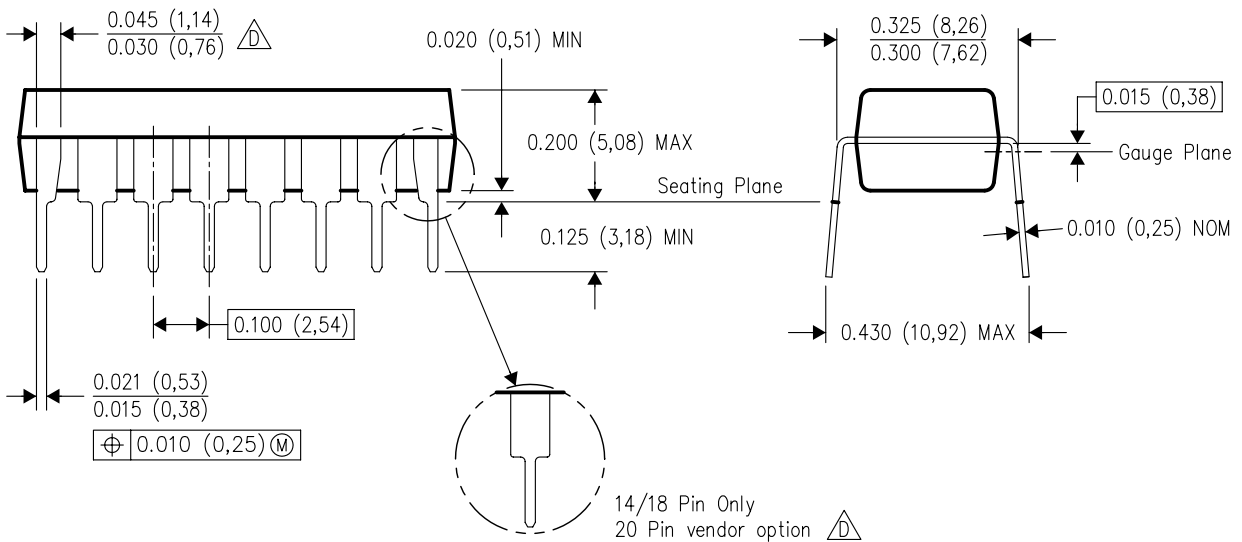
## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

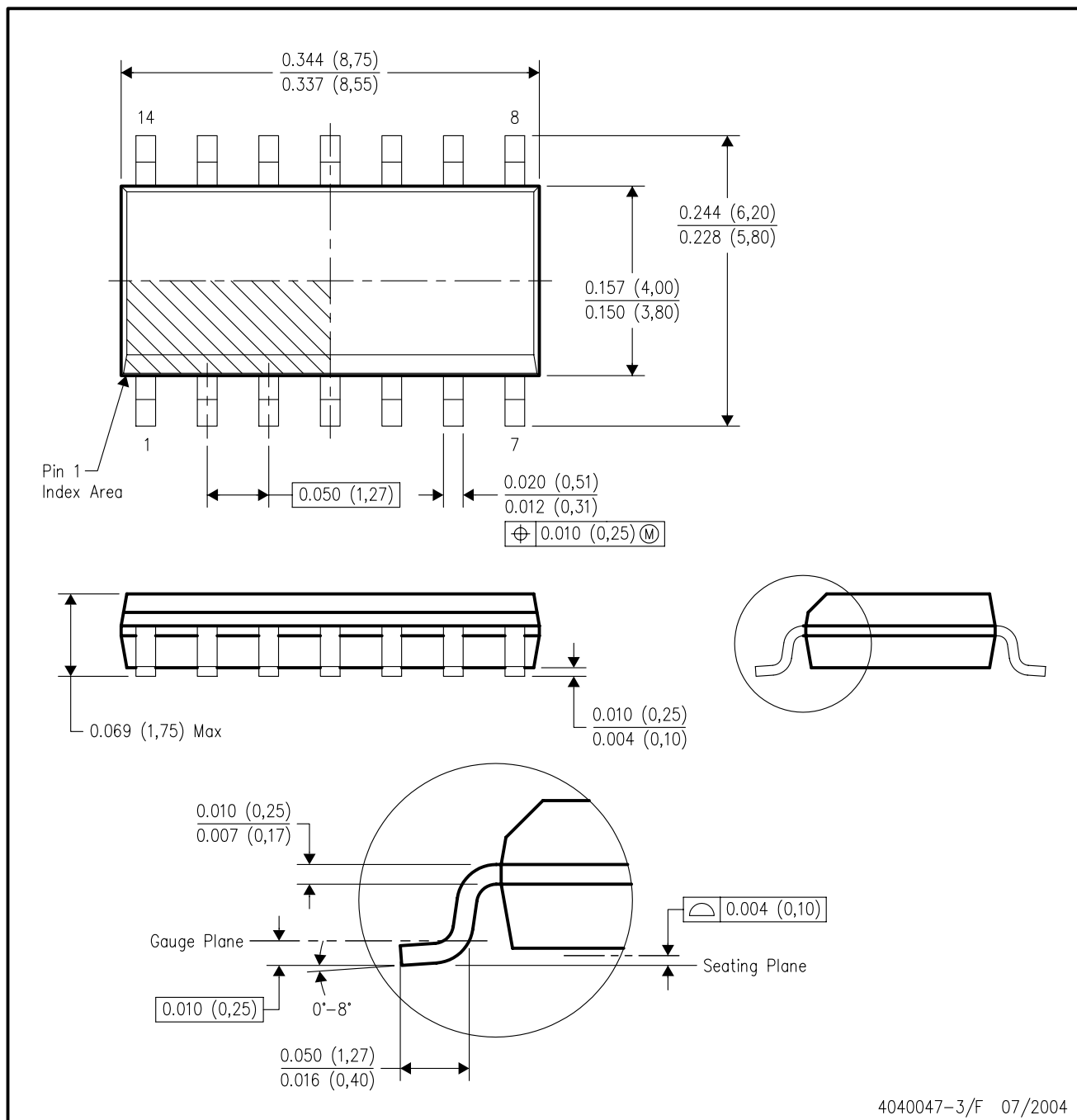


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G14)

## PLASTIC SMALL-OUTLINE PACKAGE



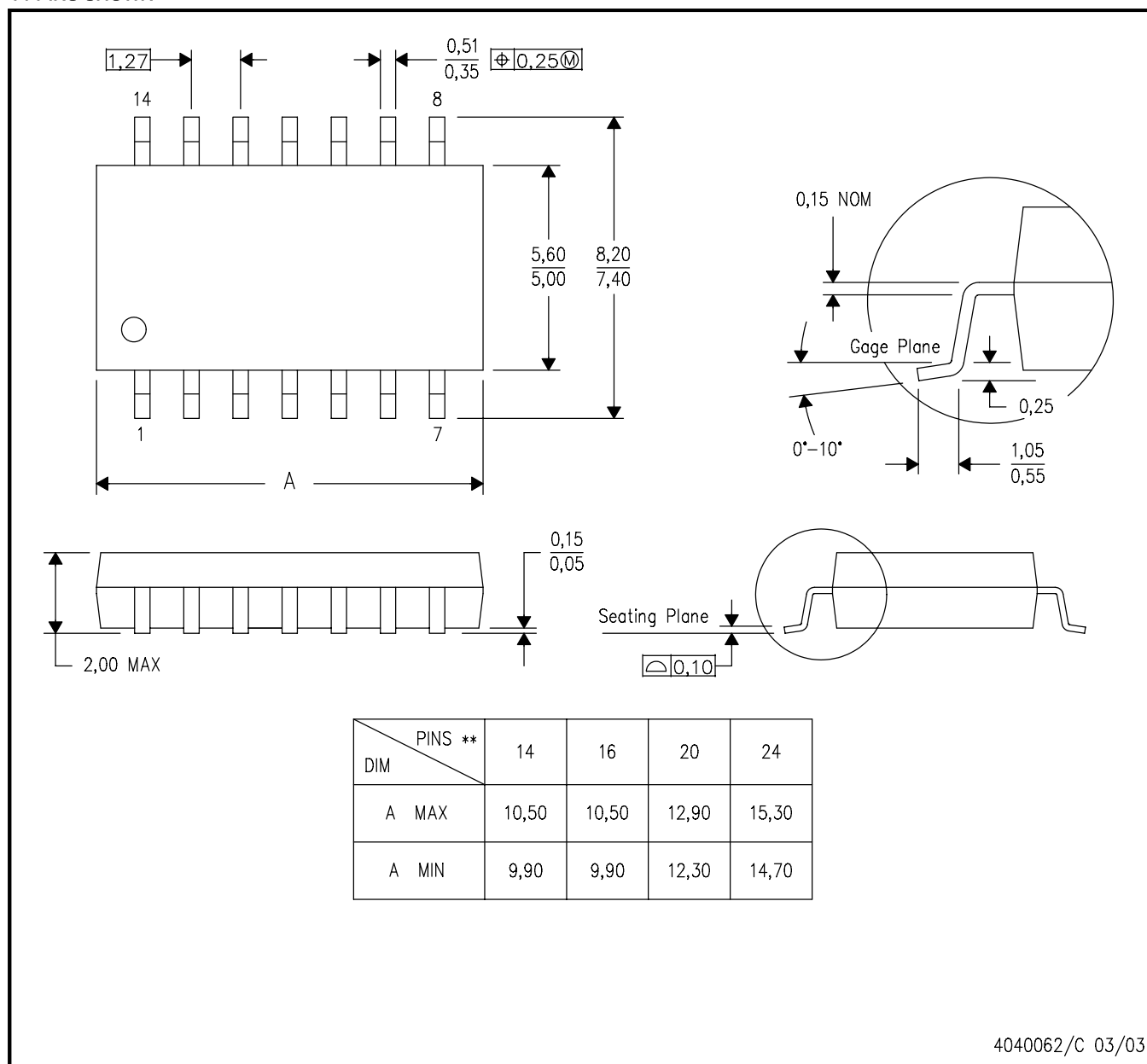
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# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

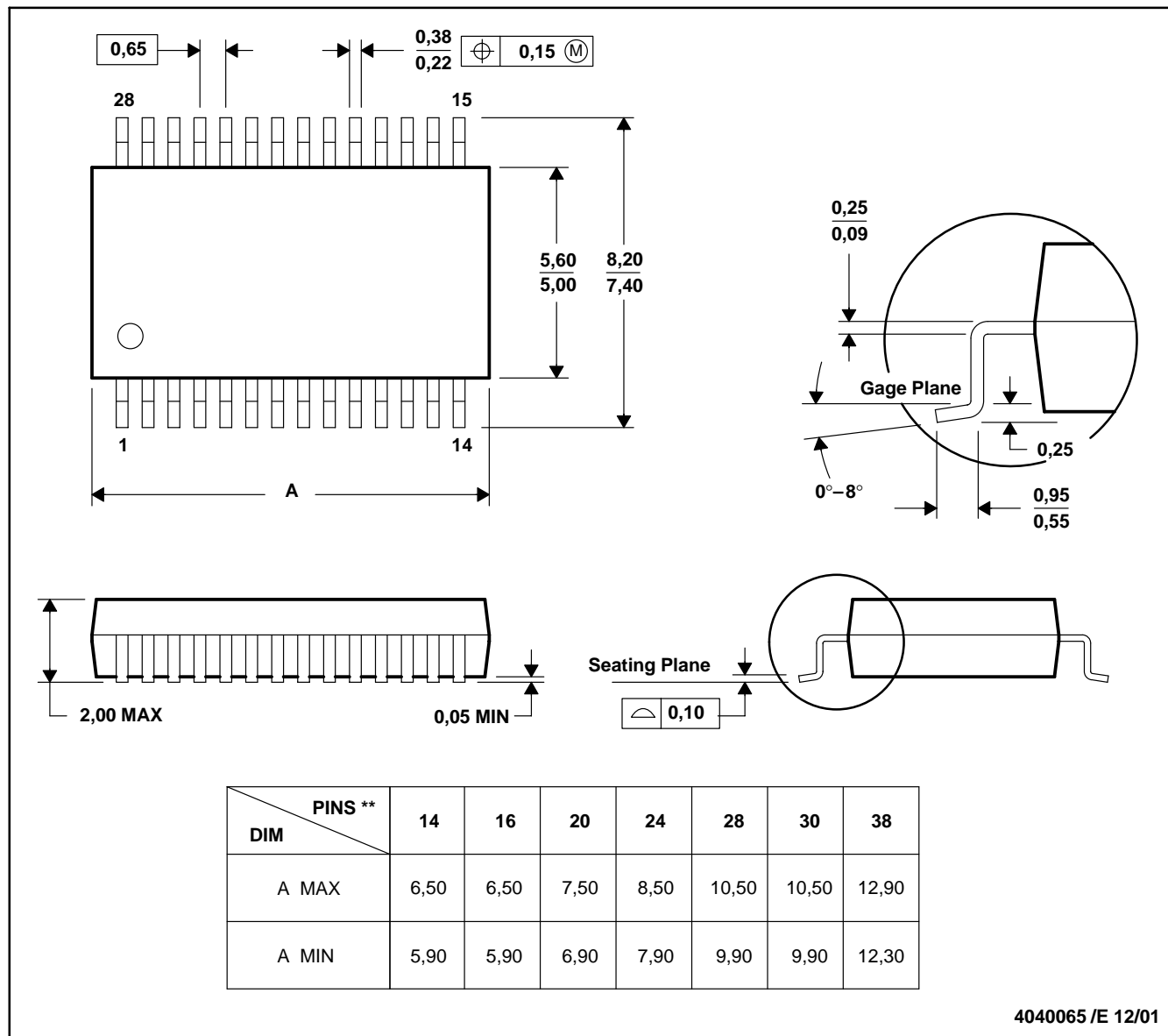


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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