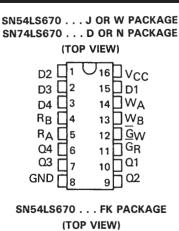
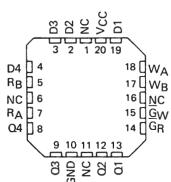
- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- For Use as:
 - Scratch-Pad Memory Buffer Storage between Processors Bit Storage in Fast Multiplication Designs
- 3-State Outputs
- SN54LS170 and SN74LS170 Are Similar But Have Open-Collector Outputs



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description

The SN54LS670 and SN74LS670 MSI 16-bit TTL register files incorporate the equivalent of 98 gates. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

NC - No internal connection.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write-address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, \overline{G}_W , is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, \overline{G}_R , is high, the data outputs are inhibited and go into the high-impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 nanoseconds typical) and the read time (24 nanoseconds typical). The register file has a nondestructive readout in that data is not lost when addressed.

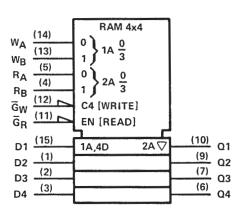
All inputs except read enable and write enable are buffered to lower the drive requirements to one Series 54LS/74LS standard load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and have high-sink-current, three-state outputs. Up to 128 of these outputs may be bus connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54LS670 is characterized for operation over the full military temperature range of -55° C to 125° C; the SN74LS670 is characterized for operation from 0° C to 70° C.



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logic symbol[†]



 $^\dagger This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.$

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD				
WB	WA	Ğ₩	0	1	2	3	
L	L	L	Q = D	Q ₀	00	0 ₀	
L	н	L	Q0	Q = D	Q ₀	0 ₀	
н	L	L	Q0	00	Q = D	0 ₀	
н	н	L	0 ₀	0 ₀	0 ₀	Q = D	
×	х	н	0 ₀	0 ₀	Q ₀	Q ₀	

READ FUNCTION TABLE (SEE NOTES A AND D)

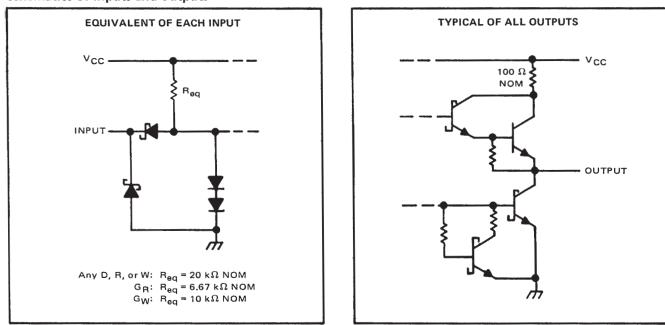
READ INPUTS			OUTPUTS				
RB	RA	GR	01	Q2	Q3	Q4	
L	L	L	W0B1	W0B2	W0B3	WOB4	
L	н	L	W1B1	W1B2	W1B3	W1B4	
н	L	L	W2B1	W2B2	W2B3	W2B4	
н	н	L	W3B1	W3B2	W3B3	W3B4	
×	x	н	z	z	z	Z	

NOTES: A. H = high level, L = low level, X = irrelevant, Z = high impedance (off)

B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

C. Q_0 = the level of Q before the indicated input conditions were established.

D. WOB1 = The first bit of word 0, etc.

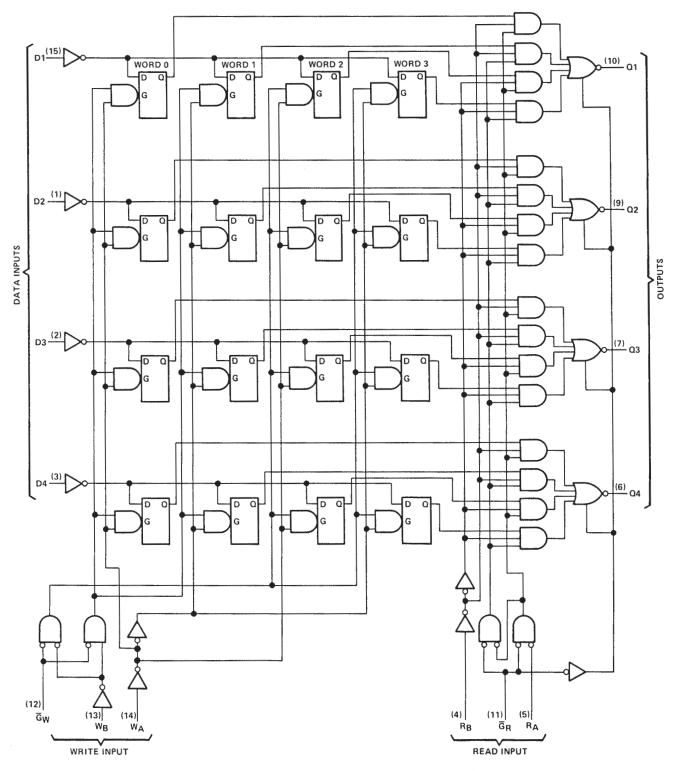


schematics of inputs and outputs



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logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)	7 V
Input voltage	7 V 1
Off-state output voltage	5 V
Operating free-air temperature range: SN54LS670	ъ°С
SN74LS670)°C
Storage temperature range	Ĵ°С

recommended operating conditions

		SN54LS670		SN74LS670				
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH				1			-2.6	mA
Low-level output current, IOL				4			8	mA
Width of write-enable or read-enable pulse, ${\rm t}_{\rm W}$		25			25			ns
Setup times, high- or low-level data	Data input with respect to write enable, t _{su} (D)	10			10			ns
(see Figure 2)	Write select with respect to write enable, t _{su} (W)	15			15			ns
Hold times, high- or low-level data	Data input with respect to write enable, t _h (D)	15			15			ns
(see Note 2 and Figure 2)	Write select with respect to write enable, th(W)	5			5			ns
Latch time for new data, tlatch (see Note 3)		25			25			ns
Operating free-air temperature range, TA		-55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.

2. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, t_{su(W)} can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during t_{h(W)} will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

3. Latch time is the time allowed for the internal output of the latch to assume the state of new data. See Figure 2. This is important only when attempting to read from a location immediately after that location has received new data.



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		TECT CONDITIONS		SN54LS670			SN74LS670				
	PARAMETER	TEST CONDITIONS [†]		MIN	TYP‡	MAX	MIN	түр‡	MAX	UNIT	
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.7			0.8	V
VIK	Input clamp voltage	V _{CC} = MIN,	I _I =18 mA				-1.5			-1.5	V
Vон	High-level output voltage	V _{CC} = MIN,	V _{IH} = 2 V,	I _{OH} = -1 mA	2.4	3.4					v
VОН	ringii-level output voltage	$V_{IL} = V_{IL} \max$		$I_{OH} = -2.6 \text{ mA}$				2.4	3.1		v
Voi	Low-level output voltage	V _{CC} = MIN,	V _{IH} = 2 V,	I _{OL} = 4 mA		0.25	0.4		0.25	0.4	v
*UL	Low-level output voltage	VIL = VIL max		IOL = 8 mA					0.35	0.5	ľ
lоzн	Off-state output current, high-level voltage applied	V _{CC} = MAX,	V _{IH} = 2 V,	V _O = 2.7 V			20			20	μA
IOZL	Off-state output current, low-level voltage applied	V _{CC} = MAX,	V _{1H} = 2 V,	V _O = 0.4 V			-20			-20	μA
	Input current at	V _{CC} = MAX,	Any D, R, or	W			0.1			0.1	
Ч	maximum input voltage		G _W				0.2			0.2	mA
	maximum input voltage	V ₁ = 7 V	ĞR				0.3			0.3	1
		Vcc = MAX,	Any D, R, or	W			20			20	
Чн	High-level input current		G _W				40			40	μA
		V ₁ = 2.7 V	Ğ _R				60			60	
		V _{CC} = MAX,	Any D, R, or	W			-0.4			-0.4	
ΗL	IL Low-level input current	$V_{1} = 0.4 V$	G _W				-0.8			-0.8] mA
		-	GR				-1.2			1.2	
los	Short-circuit output current§	V _{CC} = MAX			-30		-130	-30		-130	mA
ICC	Supply current	V _{CC} = MAX,	See Note 4			30	50		30	50	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at V_{CC} = 5 V, T_A = 25° C.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

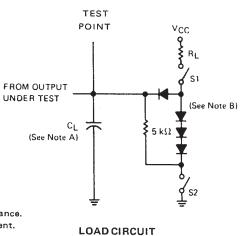
NOTE 4: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded and all outputs are open.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25^{\circ}C$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	MAX	UNIT
^t PLH	Read select	Any Q	$C_L = 15 pF$, $R_L = 2 k\Omega$,		23	40	
tPHL		Any Q	See Figures 1 and 2		25	45	ns
^t PLH	Write enable	Any Q			26	45	ns
^t PHL	Wille enable	Any d	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Figures 1 and 3		28	50	115
tPLH	Data	Any Q			25	45	ns
tPHL					23	40	1 115
^t PZH		Any Q	C _L = 15 pF, R _L = 2 kΩ,		15	35	ns
^t PZL	Read enable		See Figures 1 and 4		22	40	- 115
^t PHZ			$C_L = 5 pF$, $R_L = 2 k\Omega$,	30	50		
tplz			See Figures 1 and 4		16	35	ns



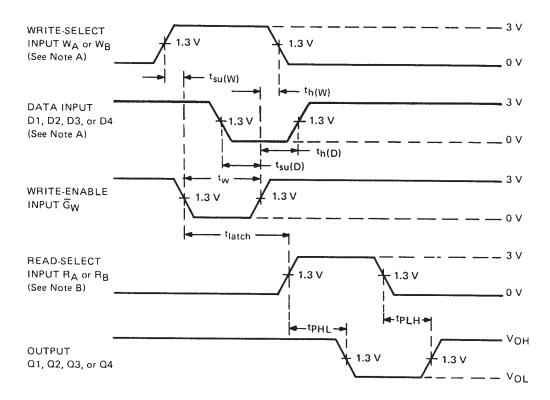
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PARAMETER MEASUREMENT INFORMATION

NOTES: A. Ct includes probe and jig capacitance. B. All diodes are 1N3064 or equivalent.

FIGURE 1



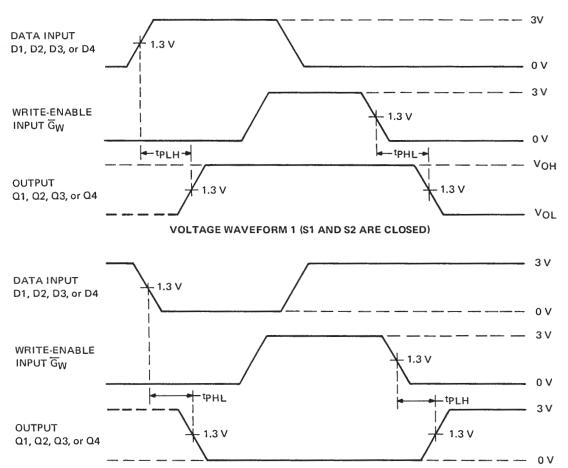
VOLTAGE WAVEFORMS (S1 AND S2 ARE CLOSED)

- NOTES: A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.
 - B. When measuring delay times from a read-select input, the read-enable input is low.
 - C. Input waveforms are supplied by generators having the following characteristics: PRR \leq 2 MHz, Z_{out} \approx 50 Ω , duty cycle \leq 50%, t_r \leq 15 ns, t_r \leq 6 ns.

FIGURE 2



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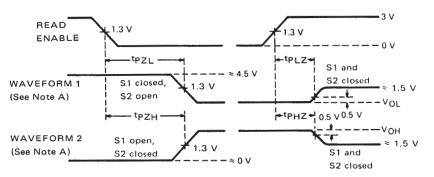


PARAMETER MEASUREMENT INFORMATION

VOLTAGE WAVEFORM 2 (S1 AND S2 ARE CLOSED)

- NOTES: A. Each select address is tested. Prior to the start of each of the above tests both write and read address inputs are stabilized with $W_A = R_A$ and $W_B = R_B$. During the test G_R is low. B. Input waveforms are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_{out} \approx 50 \Omega$, duty cycle $\leq 50\%$,
 - $t_r \leq 15 \text{ ns}, t_r \leq 6 \text{ ns}.$

FIGURE 3



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

- NOTES: A. Waveforms 1 is for an output with internal conditions such that the output is low except when disabled by the read-enable input. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the read-enable input.
 - B. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.
 - C. Input waveforms are supplied by generators having the following characteristics: PRR \leq 1 MHz, Z_{out} \approx 50 Ω , duty cycle \leq 50%,
 - $t_r \leq 15$ ns, $t_r \leq 6$ ns.

FIGURE 4



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Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
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Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

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Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
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TEXAS INSTRUMENTS www.ti.com

18-Sep-2008

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	n MSL Peak Temp ⁽³⁾
5962-7704201VEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-7704201VFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
5962-7704201VFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
7704201EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
7704201EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
7704201FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
7704201FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54LS670J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS670J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS670D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS670N	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS670N3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI
SN74LS670N3	OBSOLETE	PDIP	Ν	16		TBD	Call TI	Call TI
SN74LS670NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS670NE4	ACTIVE	PDIP	Ν	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS670NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LS670NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS670NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54LS670FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS670FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS670J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS670J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS670W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS670W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

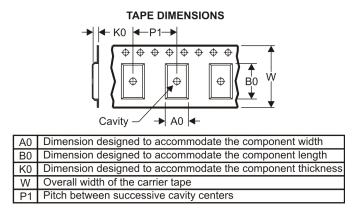
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION





QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal												
Device	•	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS670DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS670NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1



PACKAGE MATERIALS INFORMATION

19-Mar-2008



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS670DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS670NSR	SO	NS	16	2000	346.0	346.0	33.0

MLCC006B - OCTOBER 1996

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. The terminals are gold plated.
- E. Falls within JEDEC MS-004



MECHANICAL DATA

PLASTIC SMALL-OUTLINE PACKAGE

0,51 0,35 ⊕0,25⊛ 1,27 8 14 0,15 NOM 5,60 8,20 5,00 7,40 \bigcirc Gage Plane ₽ 0,25 7 1 1,05 0,55 0-10 Δ 0,15 0,05 Seating Plane — 2,00 MAX 0,10PINS ** 14 16 20 24 DIM 10,50 10,50 12,90 15,30 A MAX A MIN 9,90 9,90 12,30 14,70 4040062/C 03/03

NOTES: A. All linear dimensions are in millimeters.

NS (R-PDSO-G**)

14-PINS SHOWN

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



J (R-GDIP-T**) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AC.



D(R-PDSO-G16)



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Refer to IPC7351 for alternate board design.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- \triangle The 20 pin end lead shoulder width is a vendor option, either half or full width.



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Interface	interface.ti.com	Military	www.ti.com/military
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Microcontrollers	microcontroller.ti.com	Telephony	www.ti.com/telephony
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